100GBASE-SR4 QSFP28 Active Optical Cable

Description

100GBASE-SR4 QSFP28 Active Optical Cable is a Four-Channel, Pluggable, Parallel, Fiber-Optic QSFP+ SR4 for 100 or 40 Gigabit Ethernet , Infiniband FDR/EDR and 32GFC Applications. This transceiver is a high performance module for short-range multi-lane data communication and interconnect applications. It integrates four data lanes in each direction with 112.2 Gbps bandwidth. Each lane can operate at 28.05Gbps up to 70 m using OM3 fiber or 100 m using OM4 fiber. These modules are designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The electrical interface uses a 38 contact edge type connector. The optical interface uses an 12 fiber MTP (MPO) connector.

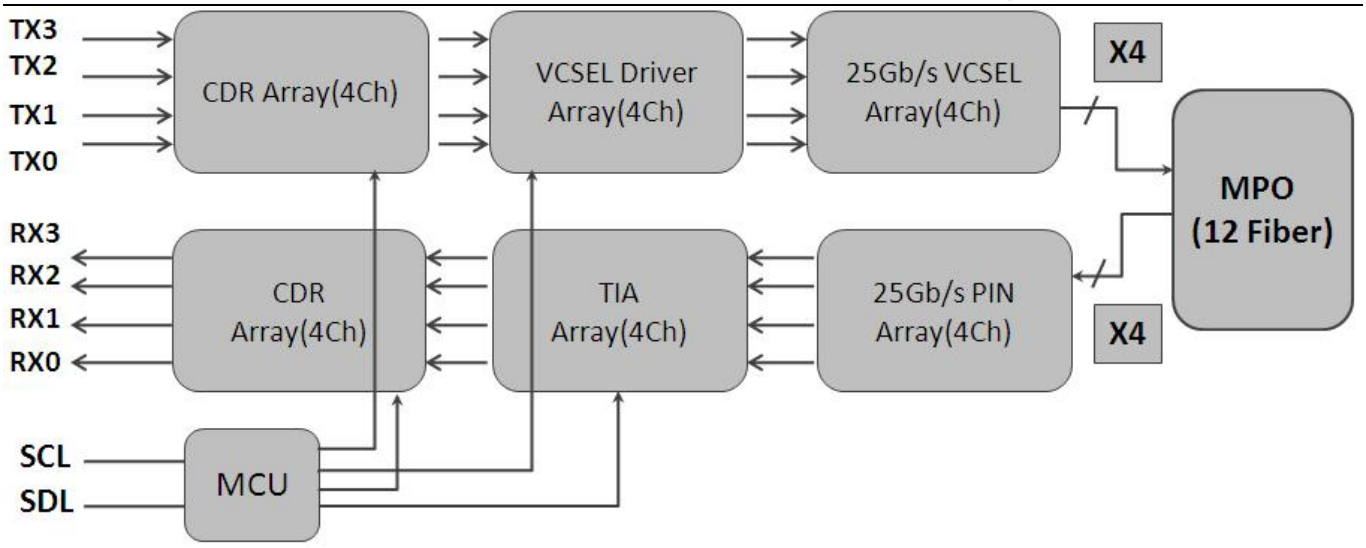
Features (Low Power Version)

- Bandwidth density of 100 Gbps bi-directional
- Transmission data rate up to 25.8Gbps per channel
- 4 channels 850nm 25G VCSEL array
- 4 channels 25G PIN photo detector array
- Internal CDR circuits on both receiver and transmitter channels
- Hot Pluggable QSFP28 form factor
- Maximum link length of 70m on OM3 Multimode Fiber (MMF) and 100m on OM4 MMF
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- Low power consumption <2.5W
- RoHS 6 compliant(lead free)

Applications

- IEEE 802.3bm 100GBASE SR4
- InfiniBand EDR
- Datacom/Telecom switch & router connections
- Data Aggregation and Backplane Applications
- Proprietary Protocol and Density Applications

SHENZHEN TRANSCOM TECHNOLOGY LIMITED / 303, Building 4, Fantasia MIC Plaza,Nanshan District,Shenzhen,China.



* 100GBASE-SR4 QSFP28 is one kind of parallel transceiver. VCSEL and PIN array package is key technique, through I2C system can contact with module.

Absolute Maximum Ratings

Parameter	**Symbol**	**Min**	**Max**	**Unit**
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	ºC
Case Operating Temperature	Top	0	70	ºC
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	ºC
Data Rate Per Lane	fd	25.78125		28.05	Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm	2		2.5	W
Fiber Bend Radius	Rb	3			cm

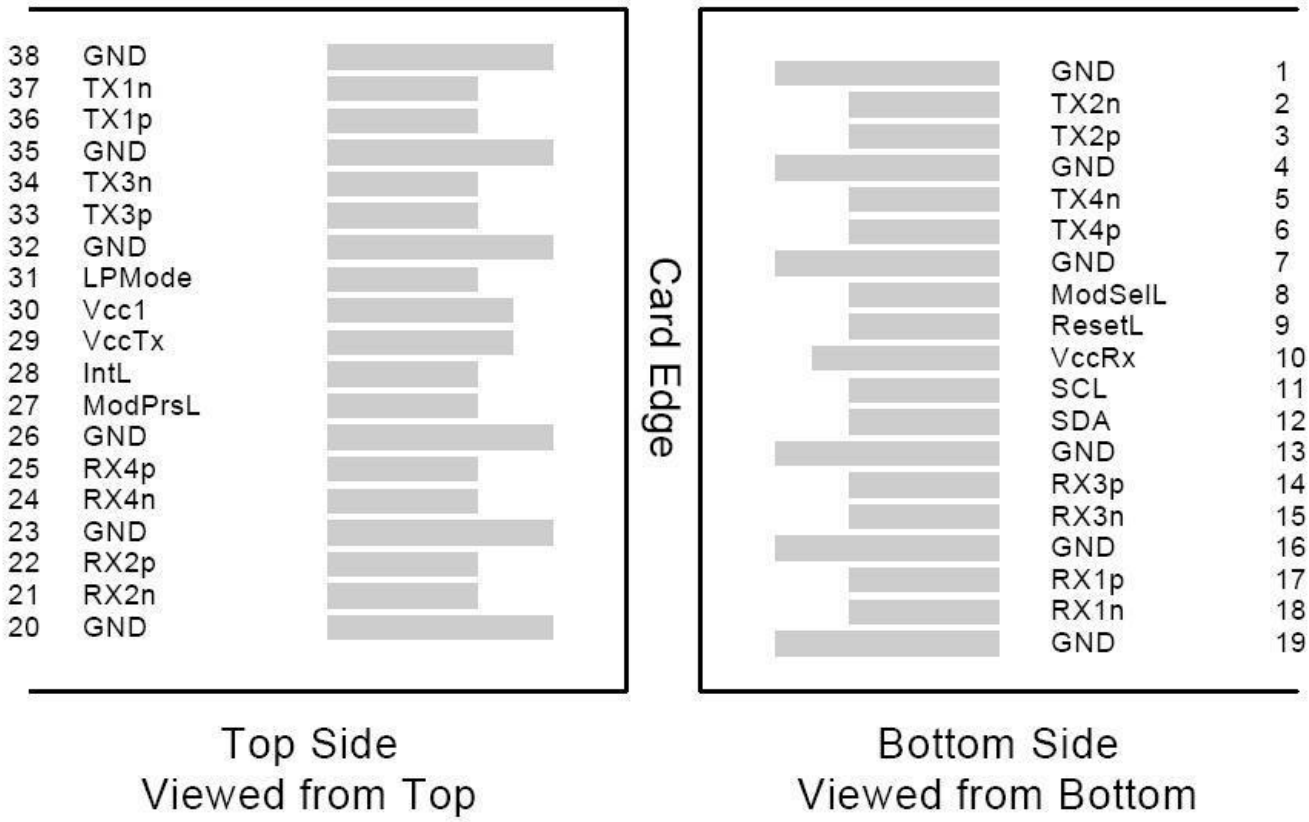
Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude aAmplitude	ΔVin	300	1100		mVp-p
Differential output voltage amplitude	ΔVout	500	800		mVp-p
Skew	Sw	300			ps
Bit Error Rate	BER	E-12			
Input Logic Level High	VIH	2.0	VCC		V
Input Logic Level Low	VIL	0	0.8		V
Output Logic Level High	VOH	VCC-0.5	VCC		V
Output Logic Level Low	VOL	0	0.4		V

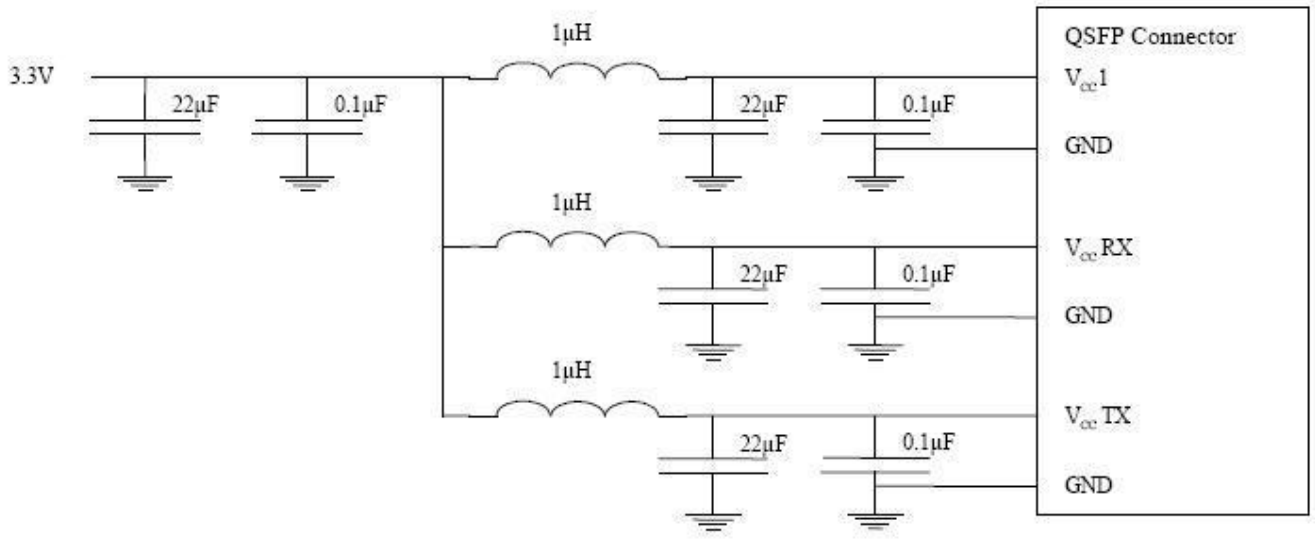
Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λc	840	850	860	nm	-
RMS spectral width	Δλ	-	-	0.6	nm	-
Average launch power, each lane	Pout	-8.4	-	2.4	dBm	-
Optical Modulation	OMA	-6.4	3	dBm		-

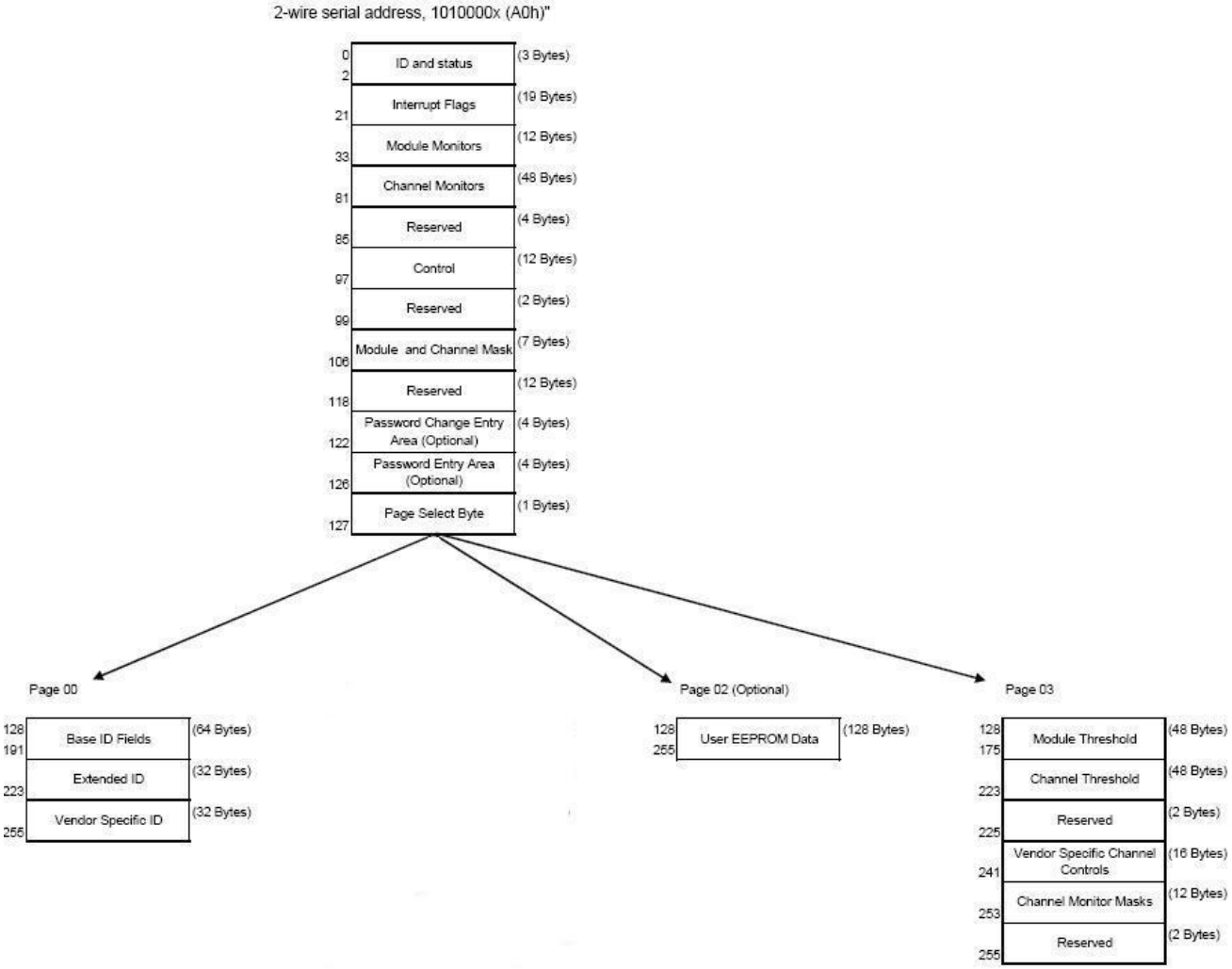
Amplitude (OMA),each lane					
Transmitter and dispersion eye closure(TDEC),each lane	TDEC		4.3		dB
Extinction Ratio	ER	3	-	-	dB	-
Average launch power of OFF transmitter, each lane	-30		dB		-
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3	SPECIFICATION VALUES {0.3,0.38,0.45,0.35,0.41.0.5}		Hit Ratio = 5x10-5		
Receiver					
Centre Wavelength	λc	840	850	860	nm	-
Stressed receiver sensitivity in OMA	-5.2		dBm		1
Maximum Average power at receiver , each lane input, each lane	2.4		dBm		-
Minimum Average power at receiver , each lane	-10.3		dBm		



Electrical Pin-out Details



Host Board Power Supply Filtering

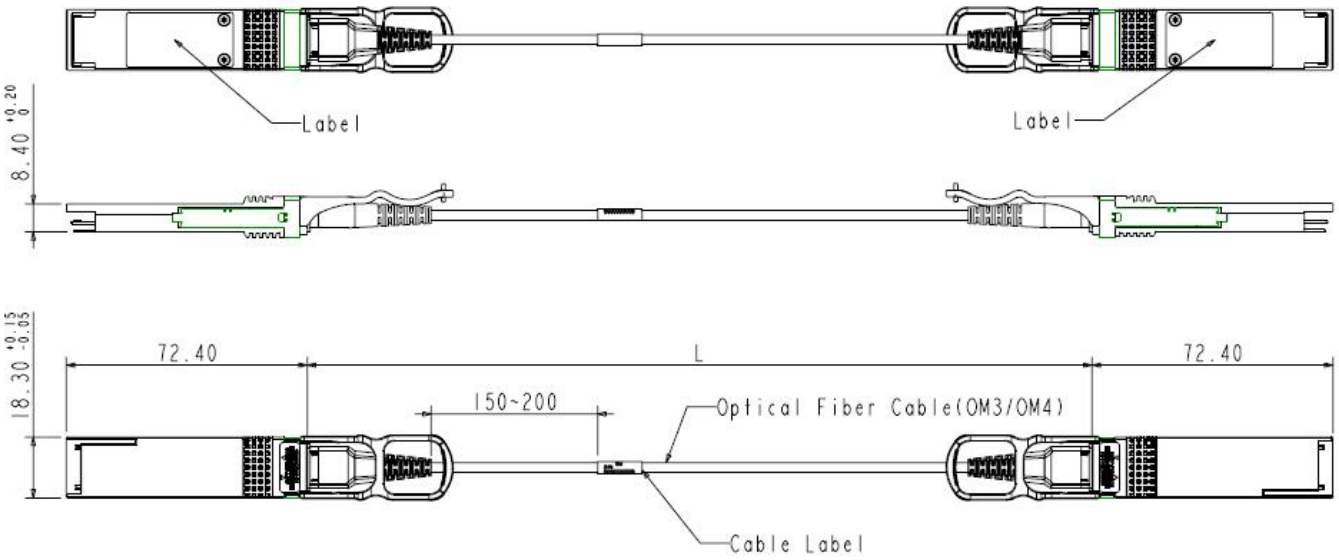


QSFP Memory Map

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on1, hot plug or rising edge of Reset until the module is fully functional2
Reset Init Assert Time	t_reset_init	2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on1 until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on1 to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional2

LPMode Assert Time	ton_LPMode	100	μs	Time from assertion of LPMode (Vin:LPMode = Vih) until module power consumption enters lower Power Level
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL Deassert Time	toff_IntL	500	μs	Time from clear on read3 operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set4 until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared4 until associated IntlL operation resumes
ModSelL Assert Time	ton_ModSelL	100	μs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus
ModSelL Deassert Time	toff_ModSelL	100	μs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set 4 until module power consumption enters lower Power Level
Power_over-ride or Power-set Deassert	toff_Pdown	300	ms	Time from P_Down bit cleared4 until the module

Timing for Soft Control and Status Functions



Mechanical Dimensions