QSFP Active Optical Cable

Description

QSFP Active Optic Cables are a high performance, low power consumption, long reach interconnect solution supporting InfiniBand FDR/QDR/DDR/SDR,16G/10G/8G/4G/2G fiber channel , PCIe and SAS. It is compliant with the QSFP MSA and IEEE P802.3ba 40GBASE-SR4. QSFP AOC is an assembly of 4 full-duplex lanes, where each lane is capable of transmitting data at rates up to 14.025Gb/s, providing an aggregated rate of 56Gb/s.

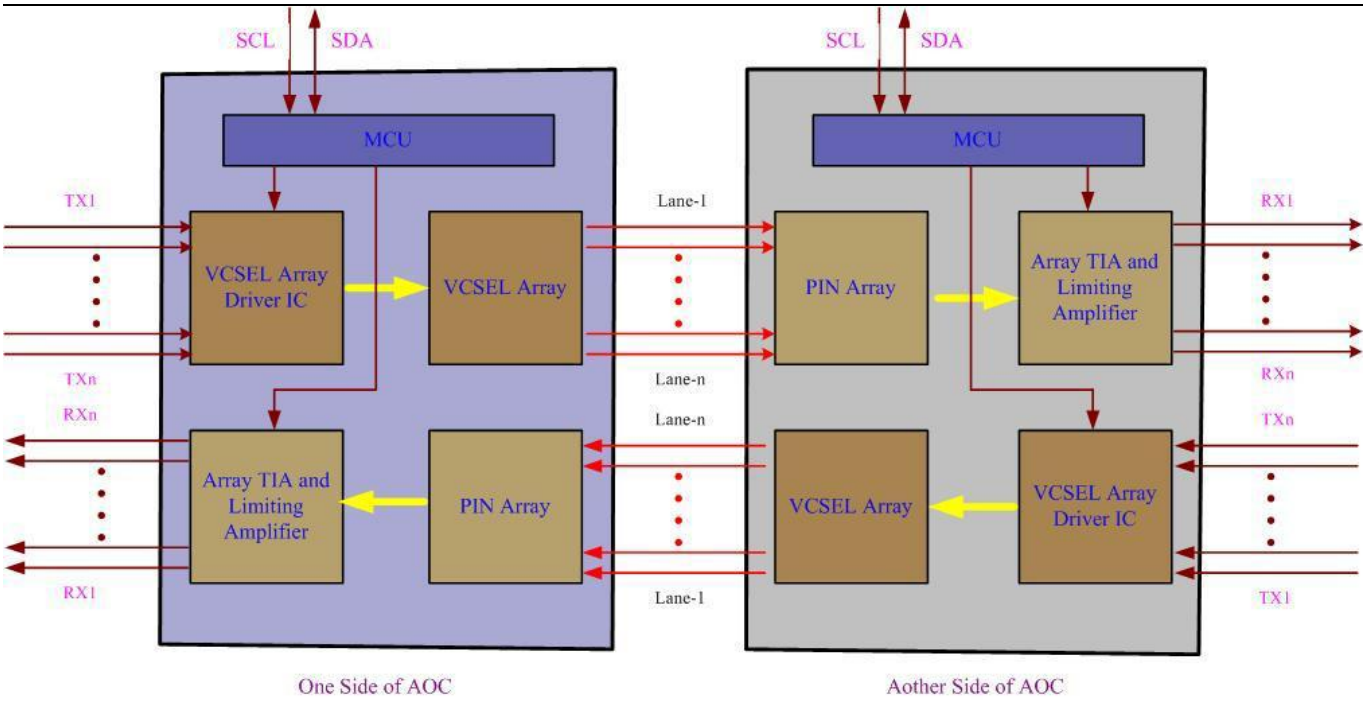
Features

- Full duplex 4 channel 850nm parallel active optical cable
- Transmission data rate up to 14.025Gbit/s per channel
- SFF-8436 QSFP+ compliant
- Hot pluggable electrical interface
- Differential AC-coupled high speed data interface
- 4 channels 850nm VCSEL array
- 4 channels PIN photo detector array
- Maximum link length of 100m on OM3 Multimode Fiber (MMF)and 150m on OM4 MMF
- Low power consumption
- Housing isolated from connector ground
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- RoHS 6 compliant

Applications

- InfiniBand FDR
- 16x Fibre Channel
- PCI-e3.0
- Proprietary High Speed Interconnections
- SAS 3.0

Module Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	ºC
Case Operating Temperature	Top	0	70	ºC
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	ºC
Data Rate Per Lane	fd	2.5		14.025	Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm		1.5		W
Fiber Bend Radius	Rb		3		cm

Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential	Zout	90	100	110	ohm

Output impedance					
Differential input voltage amplitude aAmplitude	ΔVin	300	1100	mVp-p	
Differential output voltage amplitude	ΔVout	500	800	mVp-p	
Skew	Sw	300	ps		
Bit Error Rate	BR	E-12			
Input Logic Level High	VIH	2.0	VCC	V	
Input Logic Level Low	VIL	0	0.8	V	
Output Logic Level High	VOH	VCC-0.5	VCC	V	
Output Logic Level Low	VOL	0	0.4	V	

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λc	840	850	860	nm	-
RMS spectral width	Δλ	-	-	0.65	nm	-
Average launch power, each lane	Pout	-7.5	-	2.5	dBm	-
Difference in launch power between any two lanes (OMA)		4		dB		-
Extinction Ratio	ER	3	-	-	dB	-
Peak power, each lane		4		dBm		-
ransmitter and dispersion penalty (TDP), each lane	TDP		3.5		dB	-
Average launch power of OFF transmitter, each lane		-30		dB		-
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3		SPECIFICATION VALUES 0.23, 0.34, 0.43, 0.27, 0.35, 0.4			Hit Ratio = 5x10-5	
Receiver						
Centre Wavelength	λc	840	850	860	nm	-
Stressed receiver sensitivity in OMA, each lane		-5.4		dBm		1
Maximum Average power at receiver input, each lane		2.4		dBm		-

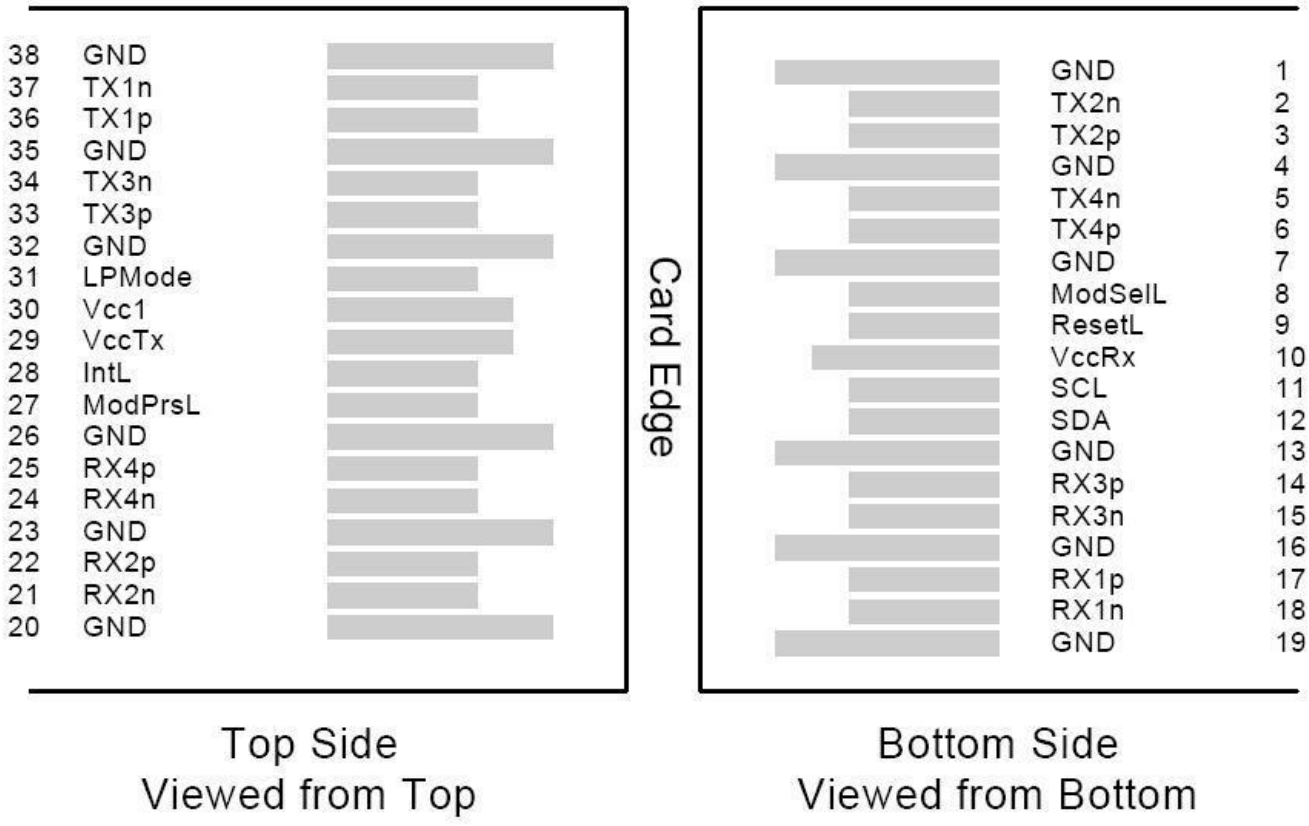
Receiver Reflectance	-12	dB	-

Pin Descriptions

Pin	Logic	Symbol	Name/Description	Ref.
1	GND	Module Ground		1
2	CML-I	Tx2-		Transmitter inverted data input
3	CML-I	Tx2+		Transmitter non-inverted data input
4	GND	Module Ground		1
5	CML-I	Tx4-		Transmitter inverted data input
6	CML-I	Tx4+		Transmitter non-inverted data input
7	GND	Module Ground		1
8	LVTTL-I	MODSEIL	Module Select	2
9	LVTTL-I	ResetL	Module Reset	2
10	VCCRx		+3.3v Receiver Power Supply	
11	LVCMOS-I	SCL	2-wire Serial interface clock	2
12	LVCMOS-I/O	SDA	2-wire Serial interface data	2
13	GND	Module Ground		1
14	CML-O	RX3+		Receiver non-inverted data output
15	CML-O	RX3-		Receiver inverted data output
16	GND	Module Ground		1
17	CML-O	RX1+		Receiver non-inverted data output
18	CML-O	RX1-		Receiver inverted data output
19	GND	Module Ground		1
20	GND	Module Ground		1
21	CML-O	RX2-		Receiver inverted data output
22	CML-O	RX2+		Receiver non-inverted data output
23	GND	Module Ground		1
24	CML-O	RX4-		Receiver inverted data output
25	CML-O	RX4+		Receiver non-inverted data output
26	GND	Module Ground		1
27	LVTTL-O	ModPrsL		Module Present, internal pulled down to GND
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board	2
29	VCCTx		+3.3v Transmitter Power Supply	
30	VCC1		+3.3v Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	2
32	GND	Module Ground		1

33	CML-I	Tx3+	Transmitter non-inverted data input
34	CML-I	Tx3-	Transmitter inverted data input
35	GND	Module Ground	1
36	CML-I	Tx1+	Transmitter non-inverted data input
37	CML-I	Tx1-	Transmitter inverted data input
38	GND	Module Ground	1

Electrical Pin-out Details



ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is “High”, the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

QSFP AOC operate in the low power mode (less than 1.5 W power consumption) This pin active high will

decrease power consumption to less than 1W

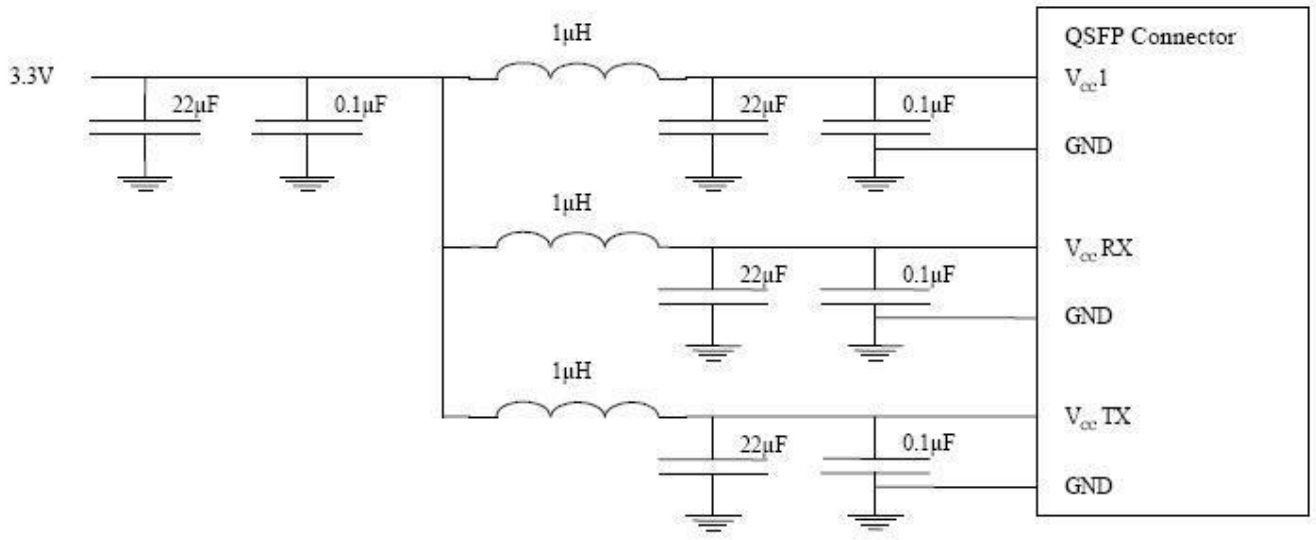
ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and deasserted “High” when the module is physically absent from the host connector.

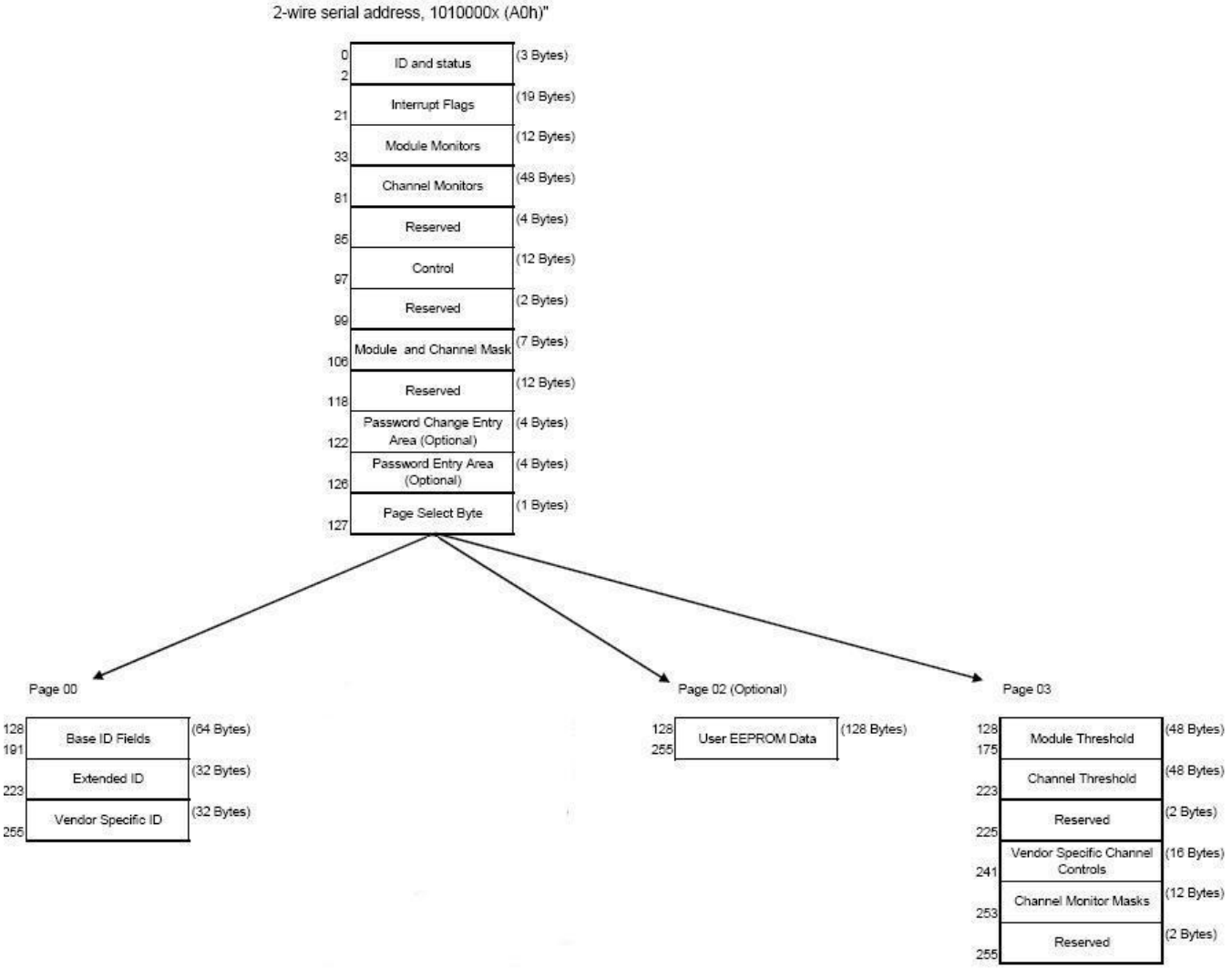
IntL Pin

IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Host Board Power Supply Filtering



QSFP Memory Map



Mechanical Dimensions